

WE CLAIM:

1. An integrated circuit, comprising:
a processing core,
a data request pipeline having an arbiter in communication with the processing core, the data request pipeline having an external bus interface, and
a validation FUB having an input coupled to the external bus interface of the data request pipeline.
2. The integrated circuit of claim 1, wherein an output of the validation FUB is coupled to the arbiter.
3. The integrated circuit of claim 1, wherein the validation FUB comprises:
a transaction latch coupled to the external bus interface, and
a request library in communication with the transaction latch and having an output coupled to the data request pipeline.
4. The integrated circuit of claim 2, further comprising an address manipulator coupled to the transaction latch and to the request library.
5. A method of stress testing an integrated circuit, comprising:
capturing a first external bus transaction,
when a request type of the transaction matches a triggering condition, generating a data request, and
generating a harassing bus transaction based on the data request.
6. The method of claim 5, wherein the first external bus transaction and the new external bus transaction are generated by the same integrated circuit.
7. The method of claim 5, wherein the data request includes an address contained in the first external bus transaction.
8. The method of claim 5, wherein the external bus transaction includes a first cache line address in a system memory and the data request includes a second cache line address adjacent to the first cache line address.

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9. The method of claim 5, wherein the external bus transaction includes an address directed to a first portion of a cache line in a system memory and the data request includes a second cache line directed to a second portion of the cache line.

10. The method of claim 5, wherein the harassing bus transaction is generated before the first external bus transaction concludes.

11. A validation FUB in an integrated circuit adapted to capture external bus transactions and generate harassing data requests to an address contained therein.

12. The validation FUB of claim 10, comprising:
a transaction latch,
a request library in communication with the transaction latch, and
a controller in communication with the transaction latch.

13. A computer system, comprising:
a plurality of agents, each coupled to a common communication bus,
one of the agents including a validation FUB.

14. The computer system of claim 13, wherein the one agent is a processor.

15. The computer system of claim 13, wherein the one agent is a memory controller.

16. The computer system of claim 13, wherein the one agent is an IO interface.

17. The computer system of claim 13, wherein validation FUB comprises:
a transaction latch in communication with the communication bus,
a request library in communication with the transaction latch, and
a controller in communication with the transaction latch.

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18. A stress testing method for a computer system, comprising:
counting a number of external bus cycles that occur without onset of a new transaction on the external bus,
when the number meets a predetermined threshold, generating a harassing transaction on the external bus.

19. The method of claim 18, wherein the harassing transaction includes an address from a previous bus transaction having been modified to refer to an adjacent cache line.